Applying the Novel High Speed Robust Level Converter to a 12-bit Successive Approximation Analog-to-Digital Converters with Dual Supply Domain

by

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Abstract

The market growth of portable devices is increasing which means that low power circuit design in digital and mixed signal area become more popular nowadays. Power consumption is one of the challenge for portable devices while usually it can be saved significantly if we design them using low supply voltage domain. Moreover, recent research has shown that typical successive approximation register analog-to-digital converter (SAR ADC) can be scaled by lower supply voltage. However, the design complexity increases when resolution is getting higher. In this thesis work, we propose a high speed robust low voltage level converter which is applied to the design of a 12-bit SAR ADC. The ADC architecture is simple and it is designed in two supply domain. A novel level converter is introduced for which it can transform high speed clock signal without degradation of ADC performance. We show that by designing the precise analog parts of SAR ADC using thick oxide devices, design complexity can be relaxed. Simulation results demonstrate the proposed level works perfectly when it is applied to the design of a 12-bit SAR ADC.

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Key words

Analog-to-digital converters

Digital-to-analog converters

Level converter

Successive approximation register (SAR)

Comparator

Pre-amplifier

Capacitor array

Reference buffer

Bandgap reference

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List of Abbreviations

ADC	:	Analog-to-Digital Converter
CMOS	:	Complementary Metal–Oxide–Semiconductor
DAC	:	Digital-to-Analog Converter
DNL	:	Differential Nonlinearity
ENOB	:	Effective Number of Bit
FFT	:	Fast Fourier Transform
HV	:	High Voltage
LC	:	Level Converter
LSB	:	Least Significant Bit
LV	:	Level Voltage
LVLC	:	Low Voltage Level Converter
MSB	:	Most Significant Bit
MOSFET	:	Metal-Oxide-Semiconductor Field-Effect Transistor
MUX	:	Multiplexer
NMOS	:	N-channel MOSFET
OPAMP	:	Operation amplifier
PMOS	:	P-channel MOSFET
PSRR	:	Power Supply Rejection Ratio
SAR	:	Successive Approximation Register
S/H	:	Sample-and-Hold
THD	:	Total Harmonic Distortion
VLSI	:	Very Large Scale Integration

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Dedication

The author wishes to dedicate this thesis to my father and mother as well as my wife Candy. They support me so much for my studies as they give me great motivation to complete this thesis writing. Also I would like to thanks my boss Ben and colleagues as they give me the innovation for analog design.

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