Monotonic Multi-Switching Method for Ultra-Low-Voltage Energy Efficient SAR ADCs

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ABSTRACT

ANALOG to digital converters (ADCs) have distinguished themselves by the rapid pace of development in their applications such as data acquisition systems, precision industrial measurements and wireless communication systems. As ADC implementations migrate to scaled-down CMOS technologies, they also face the inevitable downscaling of power supply voltage. The reduction of supply voltage can effectively save the power consumption, because lower supply voltage could reduce more power of digital circuits. However, lower supply voltage leads to decreased input signal amplitude which makes the analog circuit design more difficult. The charge-redistribution Successive Approximation Register (SAR) ADC with relatively digitized architecture is mostly preferred in portable or battery-powered devices which become smaller, require excellent power efficiency and remain durable for longer service time.

The first part of this work introduces and compares different ADC architectures and different switching techniques for charge-redstribution SAR ADCs. In order to improve the power efficiency of DAC array, this thesis proposes two different switching methods and one of them, named monotonic multi-switching (MMS) technique, can not only reduce the switching energy but most importantly decrease the total capacitance saving the cost and area of capacitive DAC array. However, the novel method has some drawbacks related to supply voltage and comparator input common-mode variations.

Moreover, redundant decisions are discussed to solve the settling issue and then to improve the conversion speed, which is negatively influenced by the ultra-low-voltage design like lower input amplitude, smaller least significant bit (LSB) or short settling time. In particular, the compensative redundancy method is introduced in detail. While this method relaxes the settling time, its employment in previous charge-redistribution SAR ADC architectrues could bring in extra compensation capacitors which has a negative effect on

speed, and waste some switching energies in redundant decisions. Nevertheless, the novel MMS combined the compensation redundancy method could use less inserted capacitors and less energy in extra decisions. Additionally, this redundancy method relaxes the sensitivity of Vcm variation in MMS technique and has error tolerance coming form comparator input common-mode variations. Therefore, the MMS SAR ADC with compensation technique could have a good conversion speed with better power efficiency and smaller area of capacitve DAC array working on ultra-low-voltage.

The second part focues on the simulation and circuit-level design in 65nm CMOS of a 0.6V 8-bit 100MS/s monotonic multi-switching SAR ADC with three redundant decisions. The simulation results match splendidly with the theoretical expectations and circuit-level implementation validates the effectiveness in low-voltage high-speed. It is the fastest SAR ADC below 1V achieving SNDR greater than 48dB and simutaneously keeping the FoM below 24 fJ/conv.step at Nyquist rate.

KEY WORDS

Analog-to-Digital Converter

Successive-Approximation Register ADC

Ultra-Low-Voltage Design

High-Speed Design

CMOS Analog Integrated Circuits

Capacitive Switching Method

Redundancy Technique

Charge-Redistribution ADC

Capacitive DAC Array

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To

My Grandparents and maternal Grandmother

My Parents, My uncle WU LI-GEN

My GF

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LIST OF ABBREVIATIONS

ADC	:	Analog-to-Digital Converter
AFE	:	Analog Front-End
CAD	:	Computer-Aided Design
CT	:	Continuous-Time
DAC	:	Digital-to-Analog Converter
DR	:	Dynamic Range
DSP	:	Digital Signal Processing
FoM	:	Figure-of-Merit
GBW	:	Gain BandWidth
GOC	:	Gain- and Offset-Compensation
IC	:	Integrated Circuit
LVS	:	Layout versus Schematic
LSB	:	Least Significant Bit
MOS	:	Metal-Oxide Semiconductor
MUX	:	Multiplexer
MSB	:	Most Significant Bit
OPAMP	:	operational amplifier
OTA	:	Operational Transconductance Amplifier
P-CDS	:	Predictive Correlated-Double Sampling
PM	:	Phase Margin
PSRR	:	Power Supply Rejection Ratio
RF	:	Radio Frequency
ROM	:	Read-Only Memory
SC	:	Switched-Capacitor
SM	:	Switching Method
SE	:	Switching Energy
SP	:	Switching Procedure
SDM	:	Sigma-Delta modulators
SFDR	:	Spurious-Free Dynamic Range
S/H	:	Sample-and-Hold
SNDR	:	Signal-to-Noise Plus Distortion Ratio
SNR	:	Signal-to-Noise Ratio
T/H	:	Track-and-Hold
TI	:	Time Interleaved
THD	:	Total Harmonic Distortion
UGB	:	Unity-Gain Bandwidth
VCM	:	Common-Mode Voltage
VLSI	:	Very Large Scale Integration
WSN	:	Wireless Sensor Node

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