Clock-Jitter Insensitive Circuit Techniques in Continuous-Time Sigma-Delta Modulators

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Jiang Yang, Tim

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Approved by _____
Supervisor

_____
Co-Supervisor

_____

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Address: State Key Laboratory of Analog and Mixed-Signal VLSI, FST, University of Macau, Av. Padre Tomás Pereira, Taipa, Macao, China.

E-mail: jiangyangtim@gmail.com

Signature _____

Date _____

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ABSTRACT

In the recent years, wireless communications technology is developed rapidly, wide bandwidth, low power dissipations and small chip size become the main requirements to the design for the ΣΔ ADCs applied in this field. Continuous-Time (CT) ΣΔ modulators turn to a preferred candidate and are extensively utilized in wireless communication systems due to the advantages wider bandwidth, lower power, smaller silicon area, lower switching noise and implicit anti-alias filtering over the Discrete-Time (DT) counterpart.

In practical implementations, some non-idealities limit the performance of CT ΣΔ modulators which lead it to be difficult to achieve higher speed and resolution. Clock-jitter induced feedback pulse-width variation is one of the most serious problems, it can introduce feedback noise which increases In-Band-Noise (IBN) power and restricts ADC's resolution.

This thesis proposes two types of circuit techniques to achieve the clock-jitter insensitivity in the feedback of CT ΣΔ modulators. The common working mechanism is generating a jitter insensitive clock signal to control the feedback current. The difference is that one technique has the advantage of low power and easy implementation; the other technique has the insensitivity to the process variation. A design example for a 2^{nd} order 1-bit CT ΣΔ modulator used in 3G WCDMA receivers is presented. The modulator is implemented in 65nm CMOS with 1V supply. The effectiveness of the proposed jitter insensitive feedback control techniques are adopted in the designed modulator and verified by the transistor-level simulation. The designed modulator achieves 68dB SNDR with the power consumption less than 5mW. With the proposed techniques, the clock-jitter tolerance can be up to $5\%T_s$ for 10-bit ADC resolution requirement.

KEY WORDS

Continuous-Time ΣΔ Modulators

Clock-Jitter Effect

Pulse-Width Variation Insensitive Feedback

Feedback Control Generation

Threshold-Crossing Detection Technique

WCDMA Receiver

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To my parents

LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
BW	Bandwidth
CMFB	Common-Mode FeedBack
CIFB	Chain of Integrators with distributed Feed-Back
CIFF	Chain of Integrators with weighted Feed-Forward
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DFF	D-Flip-Flop
DR	Dynamic Range
DSP	Digital Signal Processing
DT	Discrete-Time
ELD	Excess-Loop Delay
FPS	Fixed Pulse Shape
GSM	Global System for Mobile
HRZ	Half-Return-to-Zero
IIT	Impulse Invariant Transform
IBN	In-Band-Noise
LSB	Least Significant Bit
MASH	Multi-stAge noise SHaping
MC	Monte Carlo
MSB	Most Significant Bit
M2M	Machine-to-Machine
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function

Op-Amp	Operational Amplifier
OSR	OverSampling Ratio
PLL	Phase Lock Loop
PP	Pulse-Position
PS	Pulse Shape
PSD	Power Spectral Density
PW	Pulse-Width
RZ	Return-to-Zero
SCR	Switched-Capacitor–Resistor
SFBW	Shaped FeedBack Waveform
SI	Switched-current
SNDR	Signal-to-Noise-and-Distortion-Ratio
SNR	Signal-to-Noise Ratio
SR	Slew Rate
STF	Signal Transfer Function
TCD	Threshold-Crossing Detection
VCO	Voltage Controlled Oscillator
WCDMA	Wideband Code Division Multiple Access
ZCD	Zero-Crossing Detector
ΣΔ	Sigma-Delta
3G	3rd Generation

TABLE OF CONTENTS

ABSTRACT III
KEY WORDS IV
ACKNOWLEDGEMENT V
LIST OF ABBREVIATIONS VII
TABLE OF CONTENTS IX
LIST OF FIGURES XII
LIST OF TABLES XVIII
CHAPTER 1 INTRODUCTION 1
1.1 RESEARCH BACKGROUND 1
1.1.1 3G WIRELESS COMMUNICATIONS 1
1.1.2 ADCS IN WCDMA RECEIVERS 4
1.2 RESEARCH MOTIVATION 5
1.3 THESIS ORGANIZATION 7
1.4 STATEMENT OF ORIGINALITY 8
CHAPTER 2 FUNDAMENTALS OF OVERSAMPLING SIGMA DELTA MODULATION 11
2.1 INTRODUCTION 11
2.2 QUANTIZATION 11
2.3 OVERSAMPLING 16
2.4 SIGMA-DELTA MODULATION 17
2.5 SECOND AND HIGHER ORDER MODULATION 21
2.6 SINGLE-STAGE AND MULTI-STAGE ΣΔ MODULATOR TOPOLOGY 25
2.6.1 SINGLE-STAGE MODULATOR 26
2.6.2 MULTI-STAGE MODULATOR 27
2.7 SUMMARY 29
CHAPTER 3 CONTINUOUS-TIME SIGMA-DELTA MODULATION 30
3.1 INTRODUCTION 30

3.2 ADVANTAGES OF CONTINUOUS-TIME ΣΔ MODULATION 30
3.3 CONVERSION OF A DT ΣΔ MODULATOR TO A CT ΣΔ MODULATOR 32
3.3.1 IMPULSE INVARIANT TRANSFORM 32
3.3.2 FEEDBACK PULSE RELATED DT-CT CONVERSION 34
3.4 IMPLICIT ANTI-ALIASING FILTERING 39
3.5 IMPLEMENTATION ISSUES IN CT ΣΔ MODULATORS 42
3.5.1 FINITE GAIN AND GBW FOR THE OP-AMP IN CT INTEGRATOR 42
3.5.2 LOOP COEFFICIENTS VARIATION 45
3.5.3 EXCESS LOOP DELAY 46
3.6 SUMMARY 49
CHAPTER 4 CLOCK-JITTER IN CT SIGMA DELTA MODULATOR 51
4.1 INTRODUCTION 51
4.2 CLOCK JITTER IN CT ΔΣ MODULATORS 51
4.3 CLOCK-JITTER EFFECT IN RECTANGULAR SINGLE-BIT FEEDBACK 53
4.4 CLOCK-JITTER EFFECT IN RECTANGULAR MULTI-BIT FEEDBACK 59
4.5 JITTER SENSITIVITY REDUCTION BY NON-RECTANGULAR FEEDBACK 61
4.6 SUMMARY 64
CHAPTER 5 FIXED PULSE SHAPE FEEDBACK CONTROL TECHNIQUE 65
5.1 INTRODUCTION 65
5.2 FPS FEEDBACK TECHNIQUE VS. SFBW FEEDBACK TECHNIQUE 66
5.3 FPS FEEDBACK TECHNIQUE I: A SIMPLE CLOCK GENERATION TECHNIQUE 69
5.3.1 PULSE-WIDTH LIMITATION IN THE EXISTED TECHNIQUE 69
5.3.2 JITTER INSENSITIVE FEEDBACK WITH EXTENDED PW 70
5.3.3 SIMULATION RESULTS 74
5.4 FIXED PULSE SHAPE FEEDBACK TECHNIQUE II: THRESHOLD-CROSSING DETECTION BASED TECHNIQUE 79
5.4.1 OPERATION PRINCIPLE OF THRESHOLD-CROSSING DETECTION (TCD) TECHNIQUE 80
5.4.2 TCD TECHNIQUE USED IN RESISTIVE FEEDBACK DACS 81
5.4.3 TCD TECHNIQUE USED IN CURRENT STEERING FEEDBACK DACS 87
5.4.4 DESIGN OF ZCD 93

5.4.5 Simulation Results 94
5.5 Summary 105
CHAPTER 6 DESIGN EXAMPLE OF A 2ND ORDER SINGLE-BIT CTSDM 106
6.1 Introduction 106
6.2 System Design 106
6.3 Design of CT Loop Architecture 121
6.4 Design of The CT Integrators 123
6.4.1 Design of The 1ST Stage Integrator 124
6.4.2 Design of The 2ND Stage Integrator 127
6.5 Design of 1-bit Quantizer 130
6.6 Design of Feedback DACs 131
6.7 Simulation Results 133
6.7.1 Simulation Results of Using Feedback Control Technique I 135
6.7.2 Simulation Results of Using Feedback Control Technique II 137
6.8 Summary 142
CHAPTER 7 CONCLUSION 144
7.1 Conclusion for This Thesis 144
7.2 The future Research Work 146
BIBLIOGRAPHY 148

LIST OF FIGURES

Fig. 1.1 Functions of 3G mobile phone. 2
Fig. 1.2 Developing trend of wireless communication technology. 2
Fig. 1.3 3G share of subscriptions and revenues. 3
Fig. 1.4 Module shipment of mobile communication by technology. 3
Fig. 1.5 A broadband direct-conversion receiver capable of handling multiple wireless communication standards and bandwidth. 4
Fig. 2.1 (a) Transfer curve and (b) quantization error of a uniform multi-level quantizer. 12
Fig. 2.2 Linear model for a quantizer. 13
Fig. 2.3 (a) Transfer curve and (b) quantization error of a uniform two-level quantizer. 14
Fig. 2.4 Quantization noise distribution in both Nyquist rate and oversampling quantiation. 16
Fig. 2.5 (a) Basic architecture and (b) the corresponding linear model for ΣΔ modulator. 18
Fig. 2.6 The PSDs for the quantization noise from an oversampling quantizer and a ΣΔ modulator. 19
Fig. 2.7 Linear model for a 1st order ΣΔ modulator employing DT integrator. 20
Fig. 2.8 Linear model for 2nd order ΣΔ modulator. 22
Fig. 2.9 Linear model for a 2nd order ΣΔ modulator employing DT integrator. 23
Fig. 2.10 Lth order ΣΔ modulator. 24
Fig. 2.11 SNR versus OSR for different order modulators with 1-bit quantizer. 25
Fig. 2.12 Topologies of a 5th order (a) CIFF ΣΔ modulator and (b) CIFBΣΔ modulator. 26
Fig. 2.13 Topology of 2-2 MASH ΣΔ modulator. 28
Fig. 3.1 Block diagrams for (a) DT and (b) CT ΣΔ modulator. 33
Fig. 3.2 block diagrams for the feedback loop in (a) DT and (b) CT ΣΔ modulators. 33

Fig. 3.3 Impulse responses for (a) NRZ and (b) RZ pulse.....35
Fig. 3.4 Distributed models for 1st order (a) DT – (b) CT feedback loop.....36
Fig. 3.5 Distributed models for 2nd order (a) DT - (b) CT feedback loop. 37
Fig. 3.6 Distributed models for 3rd order (a) DT - (b) CT feedback loop.....37
Fig. 3.7 Block diagrams for a 3rd order (a) DT and (b) CT ΔΣ modulator. 38
Fig. 3.8 A modified representation for CT ΣΔ modulator. 39
Fig. 3.9 A representation for the ΣΔ modulator with CT input transfer function.....40
Fig. 3.10 CT ΣΔ modulator with input anti-aliasing filtering.....40
Fig. 3.11 STF of a 2nd order CT ΔΣ modulator.....42
Fig. 3.12 Active RC integrator used in CT ΣΔ modulator.....43
Fig. 3.13 Behavioral model for (a) finite gain and (b) GBW effect. 45
Fig. 3.14 NRZ feedback pulse (a) without and (b) with ELD. 47
Fig. 3.15 Linear separation of a delayed NRZ DAC pulse. 47
Fig. 3.16 2nd order CT ΣΔ modulator with ELD effect.....48
Fig. 4.1 Clock-jitter induced (a) PW variation and (b) PP variation 52
Fig. 4.2 NRZ feedback sequence (a) without and (b) with (c) PW jitter error. 54
Fig. 4.3 Behavioral model for clock-jitter effect in NRZ feedback.....56
Fig. 4.4 NRZ feedback sequence (a) without and (b) with (c) PW jitter error. 57
Fig. 4.5 Behavioral model for clock-jitter effect in RZ feedback.....58
Fig. 4.6 Multi-bit (a) NRZ and (c) RZ feedback sequences with (b) (d) clock-jitter error.....60
Fig. 4.7 SCR feedback pulse.....62
Fig. 4.8 realization of SCR DAC.....63
Fig. 5.1 Clock-jitter effect to (a) SCR, (b) cosine-shape and (c) SCSR feedback pulse. 67
Fig. 5.2 Fixed pulse shape feedback waveform.....68
Fig. 5.3 Jitter reduced clock generation circuit by [21]. 69
Fig. 5.4 The operation waveform for the circuit in Fig. 5.3. 70
Fig. 5.5 The proposed jitter insensitive clock generation technique.....70
Fig. 5.6 Operation principle of the proposed technique.....71
Fig. 5.7 Clock-jitter effect to the operation of the proposed technique. 73
Fig. 5.8 Comparison of feedback pulse shapes.....73

Fig. 5.9 Circuit structure of D flip-flop.....74
Fig. 5.10 Circuit structure of transmission gate.....74
Fig. 5.11 Implementation of the delay enhancement loading.....75
Fig. 5.12 Simulated waveforms for (a) master clock, (b) clock generated by the method in [4] with PW = $0.4T_S$ and (c) clock generated by the method in [4] with PW = $0.5T_S$. 76
Fig. 5.13 Simulated waveform for the pulse generated by the proposed circuit. 76
Fig. 5.14 $5\%T_s$ jitter effect in the simulated waveforms of (a) the master clock, (b) the clock generated by the method in [4] with PW = $0.4T_S$ and (c) the clock generated by the method in [4] with PW = $0.5T_S$. 77
Fig. 5.15 The fail mechanism for the circuit given in Fig. 5.3. 78
Fig. 5.16 $5\%T_s$ jitter effect in the simulated waveforms of (a) master clock and (b) the clock generated by the proposed technique. 79
Fig. 5.17 (a) circuit topology, (b) control clock and (c) operating waveform of the proposed TCD technique. 80
Fig. 5.18 RC integrator with resistive feedback DAC. 81
Fig. 5.19 (a) Signal flow expression in CT ΣΔ modulator. (b) TCD resistive feedback DAC. (c) Control clocks for the TCD circuit. 82
Fig. 5.20 Operations of the TCD DAC. (a) Input of the ZCD. (b) Feedback control signal v_c. (c) Feedback current pulse. 83
Fig. 5.21 Clock-jitter effect to the feedback pulse shape. (a) Jittered master clock. (b) Control clock clk_2 for the TCD circuit. (c) Transient RC discharge curve at the input of the ZCD. (d). Feedback current pulse. 86
Fig. 5.22 (a) Feedback pulse generated by (b) the clock-jitter insensitive feedback DAC proposed in [57].....88
Fig. 5.23 Structure of the proposed TCD current steering DAC. 89
Fig. 5.24 (a) Control clocks of the proposed VCD DAC. (b) The detected voltage on the ZCD input. (c) The generated feedback pulse. 90
Fig. 5.25 Circuit implementation of the proposed VCD feedback DAC. 93
Fig. 5.26 Circuit implementation of the proposed VCD feedback DAC. 94
Fig. 5.27 Control clock generation circuit for the TCD DAC. 94

Fig. 5.28 Simulated waveforms for the TCD resistive feedback circuit shown in Fig. 5.19. (a) System clock. (b) Control clocks for the TCD circuit. (c) Discharging voltage v_a and the detecting threshold. (d) The generated feedback control signal v_c. 95
Fig. 5.29 Simulated conducting on resistance of the switch S_2. (a) Discharging voltage v_a. (b) The conducting on resistance of the switch S_2 96
Fig. 5.30 Simulated clock-jitter effect to the TCD resistive circuit. (a) clock-jitter error in the master clock. (b) Control signals for the TCD circuit. (c) Discharging voltage v_a and the detecting threshold. (d) The generated feedback control signal. 97
Fig. 5.31 300 times iteration Monte Carlo analysis for the process variation of the R_dC_d time constant. 98
Fig. 5.32 Simulated waveforms for the operating of the TCD resistive circuit with maximum R_dC_d variation. 99
Fig. 5.33 Simulated clock-jitter effect to the TCD circuit under +20% RC variation. 100
Fig. 5.34 Simulated operating waveforms for the proposed TCD current steering feedback control generation circuit. a) System clock. (b) Control clocks for the TCD circuit. (c) Discharging voltage v_a and the detecting threshold. (d) The generated feedback control signal v_c. 101
Fig. 5.35 Simulated clock-jitter effect to the TCD resistive circuit. (a) clock-jitter induced PW error in the master clock. (b) Control signals for the TCD circuit. (c) Discharging voltage v_a and the detecting threshold. (d) The generated feedback control signal. 102
Fig. 5.36 300 times iteration Monte Carlo analysis for the process variation of the C_d. 103
Fig. 5.37 Simulated waveforms for the operating of the TCD current steering circuit with maximum C_d variation. 104
Fig. 5.38 Simulated clock-jitter effect to the TCD circuit under +15% C_d variation.105
Fig. 6.1 System architecture of a 2nd order CIFB DT ΔΣ modulator. 107
Fig. 6.2 Output spectra of the design 2nd order DT ΔΣ modulator 108
Fig. 6.3 System architecture of the designed 2nd order CT ΔΣ modulator.....108

Fig. 6.4 A comparison for the output PSDs of the design CT & DT ΔΣ modulator. 109
Fig. 6.5 Statistical output swing of the 1st and 2nd stage integrator. 110
Fig. 6.6 Statistical scaled output swing of the 1st and 2nd stage integrator. 111
Fig. 6.7 Output PSD of the designed CT ΔΣ modulator using scaled coefficients....112
Fig. 6.8 Input dynamic range of the designed CT ΔΣ modulator. 113
Fig. 6.9 Behavioral model for op-amp (a) finite dc gain and (b) GBW effect. 114
Fig. 6.10 Finite dc gain requirement for the (a) 1st stage and (b) 2nd stage integrators. 115
Fig. 6.11 Comparison for the PSDs between the system with and without finite gain effect. 116
Fig. 6.12 GBW requirement for the designed CT ΔΣ modulator. 116
Fig. 6.13 Comparison for the PSDs between the system with and without finite GBW effect. 117
Fig. 6.14 System model for coefficients variation. 117
Fig. 6.15 Integrator coefficients variation effect on the forward path. 118
Fig. 6.16 Integrator coefficients variation effect on both forward and feedback path. 119
Fig. 6.17 ELD effect for the designed modulator with RZ and NRZ feedback. 120
Fig. 6.18 Clock-jitter effect in both RZ and NRZ feedback case. 121
Fig. 6.19 Loop architecture of the designed CT ΔΣ modulator with (a) current steering feedback and (b) resistive feedback. 122
Fig. 6.20 (a) Active-RC and (b) g_m-C integrators. 123
Fig. 6.21 Op-amp used in the 1st stage integrator. 125
Fig. 6.22 CMFB circuit for the 1st stage integrator. 125
Fig. 6.23 Biasing circuit for the op-amp and CMFB amp in the 1st stage integrator. 126
Fig. 6.24 (a) The op-amp in the 2nd stage integrator and (b) the biasing circuit. 128
Fig. 6.25 The dynamic comparator for the 1-bit quantizer. 130
Fig. 6.26 The output SR latch for the dynamic comparator. 131
Fig. 6.27 RC integrator with (a) resistive feedback and (b) current steering feedback. 131
Fig. 6.28 Conventional RZ feedback control generation circuit. 133

Fig. 6.29 Output PSD for the designed CT ΣΔ modulator employing conventional RZ feedback. 134
Fig. 6.30 Output PSD for the designed CT ΣΔ modulator employing conventional RZ feedback under clock-jitter effect of 1%T_s. 135
Fig. 6.31 Output PSD for the designed CT ΣΔ modulator employing the proposed jitter insensitive clock generation technique under clock-jitter effect of 1%T_s. 136
Fig. 6.32 Simulated clock-jitter tolerance of the designed CT ΣΔ modulator with the proposed jitter insensitive and the conventional feedback control technique. 137
Fig. 6.33 Simulated output PSDs of using TCD-R feedback technique under 1%T_s clock-jitter and using conventional RZ feedback without jitter effect. 138
Fig. 6.34 Comparison of the jitter tolerance for the designed CT modulator with and without the proposed TCD-R feedback technique. 138
Fig. 6.35 Simulated output PSDs of using TCD-I feedback technique under 1%T_s clock-jitter and using conventional RZ feedback without jitter effect. 139
Fig. 6.36 Comparison of the jitter tolerance for the designed CT modulator with and without the proposed TCD-I feedback technique. 140

LIST OF TABLES

Table 3.1 *s*-domain equivalences for rectangular DAC pulse for *z*-domain loop filters 36
Table 3.2 Coefficients for 1st to 3rd order CT ΔΣ modulators with rectangular feedback 38
Table 6.1 The design specifications of the 2nd order CT ΔΣ modulator. 107
Table 6.2 Coefficients of the designed CTΔΣ modulator. 109
Table 6.3 Scaled CT coefficients 111
Table 6.4 Modeled design parameters for the CTΔΣ modulator with RZ feedback..121
Table 6.5 Summary of various benefits and drawbacks of active-RC and g_m-C integrators 123
Table 6.6 Circuit parameters for the op-amp in the 1st stage 126
Table 6.7 Performances summary of the op-amp in the 1st stage 127
Table 6.8 Circuit parameters of the op-amp in the 2nd stage 129
Table 6.9 Performances summary of the op-amp in the 2nd stage 129
Table 6.10 Parameters of the 1st and 2nd stage integrators. 130
Table 6.11 Parameters of the 1st and 2nd stage resistive feedback. 132
Table 6.12 Parameters of the 1st and 2nd stage current steering feedback.....132
Table 6.13 Performance summary of the designed CT ΣΔ modulator with different types of DACs. 141
Table 6.14 Performance comparison with some other designs.....142
Table 7.1 Characteristics comparison of the proposed techniques. 146