Speed Enhancement Techniques for Comparator-Based Switched-Capacitor Circuits

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ABSTRACT

Digital integrated circuits (ICs) have been benefited comprehensively by the continuing CMOS technology scaling while analog designs experience many aspects of difficulties. Switched-Capacitor (SC) Circuits have been playing an important role in analog IC applications over the past decades. Many traditional sample-data systems mainly rely on operational amplifiers (opamp). However, the design of an opamp becomes increasingly challenging due to reduced supply voltages and low intrinsic device resistance in scaled CMOS technologies.

Recently, different classes of topologies have shown to be feasible to replace the functionality of opamp in sampled-data systems. Comparator-based switched-capacitor (CBSC) circuit technique is one of the applicable candidates to implement high performance opamp-less sampled-data applications and it is also compatible with most known architectures. Nevertheless, the conventional operation scheme in CBSC circuit technique limits its capability while operating at high speed.

This thesis will propose two speed-enhancement techniques for CBSC circuits to boost their competence at higher operating frequency. The first part of this work will explore in detail with the principle of operation of the two proposed techniques, as well as their circuit implementation. The second part will present both system-level and circuit-level design of the sigma-delta (ΣΔ) modulators incorporated with the two proposed CBSC techniques. The first ΣΔ modulator with 500 kHz signal bandwidth achieves a dynamic range (DR) of 81 dB and consumes 3 mW. The second one with 2 MHz signal bandwidth achieves a DR of 70 dB and consumes 2.8 mW. Both of them were implemented in 90 nm CMOS technology with 1.2-V voltage supply.

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