Design of Analog-to-Digital Converters with Binary Search Algorithm and Digital Calibration Techniques

by

Si Seng Wong, Dicky

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Faculty of Science and Technology
University of Macau

Abstract

ANALOG to digital converters (ADCs) act as a “translator” between the real world and the computer world, which “translate” the human known information from analog signal into digital signal for computers to process. The demanding market of the ADCs are increasing rapidly due to the broad-range of applications such as image processing, consumer electronics, bio-medical instruments, and wireless communicaiton, etc. In the recent years, the CMOS technology are scaling down in a fast trends, leading to higher speed and lower power consumption because of smaller parasitic capacitance for digital circuit design. However, reducing the channel-length of the transistors brings more challenge for analog circuit design. The design of operational amplifier (OP-AMP) becames an challenging issue due to the reductions of transistor intrinsic gain and supply voltage. On the other hand, reducing the size of the transistors leads to offset problems. Therefore, design of high-speed high resolution ADC in nanometer technology becomes a very challenging issue in the integration circuit (IC) design.

While the technology is scaling down, the power consumption and area of the digital circuits are reduced increadibly. Thus, modern mixed-signal design trends are putting more digital part instead of analog part. Digtial calibration is a technique to achieve better linearity in ADC designs. Using the foreground digital calibration techqniues, the linearity of the ADCs is enhanced without any additional power consumption because the calibration logics are switched off after the calibration process.

My research works mainly focus on the ADC architectures that are highly related on digital circuits. Within all the Nyquist rate ADC architectures, the architectures applying binary search algorithm such as binary-search ADC and successive approximation register (SAR) ADC mainly rely on the digital circuit design. This thesis presents three research works that are based on binary-search

algorithm. The first research work proposes a calibration technique for medium speed medium resolution ADC. This technique calibrates the parasitic effects on the split capacitor array, and it is a foreground calibration scheme, so it does not consume power during normal ADC operation. The calibration technique is designed and simulated under a 10-bit 100MS/s SAR ADC structure, with 15% to 25% of top plate parasitic capacitance. Detail logic flow of the calibration technique will be discussed in Chapter 2. The second research work proposes a new 5-bit 600MS/s binary-search ADC architecture designed in 65 nm CMOS process. The proposed ADC uses three different techniques, namely, distributed-residue, folding, and interleaved reference pre-charging, in order to prevent signal dependent offset, reduce the switching network complexity, and minimize the power consumption of the reference ladder. Detail implementation scheme will be discussed in Chapter 3. The last research work is a 5-bit 500MS/s binary-search ADC fabricated in 65 nm. This architecture is an improved version of the second research work, which further reduced the number of comparators from 2N-1 to N for N-bit resolution. The implementation detail together with the measurement results will be discussed in Chapter 4.

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