A Study on Comparator and Offset Calibration Techniques in High Speed Nyquist ADCs

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ABSTRACT

Gordon Moore has predicted the number of transistors on chip will be doubled about every two years from 1970 which is commonly known as Moore's Law. The development of integrated-circuit (IC) has stuck with this law by cutting the transistor dimensions in half in every two years, which greatly reduces the power consumption and cost per transistor. While technology scaling makes the digital signal processing (DSP) very powerful, it becomes a challenge in the design of high speed analog to digital interface. Especially, Nyquist analog-to-digital converters (ADCs) have to maintain the performance at high input frequency.

In most Nyquist ADCs such as Flash, SAR, Binary-Search and Pipeline, comparators are considered as a very important building block. Pipeline ADC usually relaxes the comparators design complexity by error correction and uses to be considered not important for comparator design. However, it is not true in the modern pipeline ADC design with nano-meter technology and calibration of comparator is also required. Furthermore, Flash, SAR and Binary-Search ADCs are considered as highly comparator-based ADC architectures whose performance is greatly relied on the comparators design.

In this thesis, different comparator architectures and offset calibration techniques will be described, analyzed and compared. The proposed offset calibration technique can greatly reduce the offset voltage in the comparators with small power consumption. Unlike the conventional approach, the presented technique does not require extra operation phases and amplification components which make this method suitable for high speed and low power design. Furthermore, under the analysis of different offset calibration approaches, the proposed technique improves the trade-off between calibration ranges, noise and able to achieve higher calibration resolution than the other calibration approaches. The calibration scheme and analytical results have been proven with simulation and multiple experiments. Three different ADC architectures have adopted the proposed method and achieved an expected performance during the measurement. Lastly, a design example of a high speed inverter-based Flash ADC is presented with post-layout simulation results. This ADC utilizes a similar calibration approach with modification for inverter-based Flash ADC architecture, which solves the linearity limitation comparing to the conventional inverter-based architecture.

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