High Speed Power/Area Optimized Multi-Bit/Cycle SAR ADCs

by

Wei He Gong

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University of Macau

Abstract

HIGH-PERFORMANCE Analog-to-Digital Converters (ADCs) are highly demanded by modern instrumentation, data acquisition and wire-line/wireless communication systems. However, the need of high speed is always accompanied by large power and area consumption since amplifier with large bandwidth or strong digital buffers are mandatory to fulfill the stringent requirements of high operation rate. Although the rapid down-scaling of CMOS technology raises the design challenges towards the need of high-gain amplifiers or low-noise devices, as well as increases the difficulty of implementing various ADC architectures, the Successive Approximation Register (SAR) ADCs with their highly digitalized structure exhibit immunity to such mentioned challenges.

The first part of this work summarizes the specialty and limitation of existing ADC architectures and introduces a solution, the multi-bit/cycle SAR ADC. In order to optimize the power/area induced by the multiple reference voltages, a monotonic resistive Digital-to-Analog Converter (DAC) is proposed to generate the reference voltages. Other associated circuit techniques are also implemented including the well-organized DAC switch diagram and the special inverter-configured decoder to further reduce the power and area. Linearity enhancement solutions of cross-coupled bootstrapping network and an offset calibration scheme are also addressed and a rapid dynamic bit register is shown to minimize the digital propagation delay inside the approximation period.

The second part focuses on the design and implementation in advanced 65nm CMOS of an 8-bit 400MS/s resistive DAC based SAR ADC which demonstrates to have the greatest potential for reaching the best efficiency with this architecture.

Its experimental results match splendidly with the theoretical expectations and validate the effectiveness of the presented architecture- circuit- and layout-level enhanced implementation with solving the arduous tradeoff in such high-frequency low-power operation with small-area, contributing as well for its high-efficiency. The prototype chip exhibits an excellent performance, showing so far, the lowest power consumption, smallest active area and best FOM among the state-of-the-art of all 7b+ 200MS/s ADCs. It is also the fastest SAR ADC achieving a SNDR greater than 40dB without time-interleaved structure, bringing up the successive approximation architecture to an unprecedented higher-level of specifications beyond its traditional range.

UNIVERSIDADE DE MACAU
仁義禮知信
澳門大學

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