

**Hardware Accelerated Nios II Implementation of
Hilbert Huang Transform**

基於 Nios II 軟核處理器的希爾伯特黃變換硬體加速實現

by

Wang Lei

Master of Science in Electrical and Electronics Engineering

2010



**Faculty of Science and Technology
University of Macau**

Hardware Accelerated Nios II Implementation of Hilbert
Huang Transform

基於Nios II軟核處理器的希爾伯特黃變換硬體加速實現

by

Wang Lei (M-A7-6559-2)

A thesis submitted in partial fulfillment of the
requirements for the degree of

Master of Science in Electrical and Electronics
Engineering

Faculty of Science and Technology
University of Macau

2010

Approved by _____
Supervisor

Date _____

In presenting this thesis in partial fulfillment of the requirements for a Master's degree at the University of Macau, I agree that the Library and the Faculty of Science and Technology shall make its copies freely available for inspection. However, reproduction of this thesis for any purposes or by any means shall not be allowed without my written permission. Authorization is sought by contacting the author at

Address: Biomedical Engineering Laboratory, Department of Electrical and Electronics Engineering, Faculty of Science and Technology, University of Macau, Macau S.A.R., China

Telephone: +853 8397-4276
E-mail: wanglei@eee.umac.mo

Signature _____

Date _____

University of Macau

Abstract

HARDWARE ACCELERATED NIOS II
IMPLEMENTATION OF HILBERT HUANG TRANSFORM

by Wang Lei

Thesis Supervisor: Prof. VAI Mang I & Dr. MAK Peng Un
Master of Science in Electrical and Electronics Engineering

Today, more and more people are caring about their health, so biomedical research is much more important for human being. Biomedical signal processing is one of the most important research areas in biomedical engineering, but most of the biomedical signals are nonlinear and non-stationary signals. And the traditional methods like Fourier transform are limited to the priori assumption that the signals being processed should be linear and stationary, which is a restriction for biomedical signal processing. In 1998, N. E. Huang proposed a novel algorithm which named Hilbert Huang Transform, this algorithm is very good at processing nonlinear and non-stationary signals, and it already has a lot of applications on biomedical engineering. But the huge computation cost is a bottleneck to implement those applications with real-time processing.

This thesis presents a “Fast Instantaneous Frequency Analyzer Based on Hilbert transform”, the system can analyze nonlinear and non-stationary signals such as biomedical signals in time-frequency domain with a 3D spectrum. It clearly demonstrates the process of nonlinear and non-stationary signal during changing. And this thesis also proposes a method to use the concept of System On Programmable Chip to combine the soft-core processor with hardware functions to implement the acceleration for Hilbert Huang Transform. After evaluation, this method is proved to be effective.

TABLE OF CONTENTS

| | |
|---|-----|
| List of Figures | iii |
| List of TABLES | v |
| LIST of Abbreviations | vi |
| Chapter 1: Introduction..... | 1 |
| 1.1 Background and Motivation | 1 |
| 1.2 Releated Works of Biomedical Data Processing Using HHT | 2 |
| 1.3 Statement Originally | 4 |
| 1.4 Thesis Origation..... | 5 |
| Chapter 2: Hilbert Huang Transform..... | 6 |
| 2.1 Instantaneous Frequency | 6 |
| 2.2 Intrinsic Mode Function | 7 |
| 2.3 Empirical Mode Decomposition..... | 8 |
| 2.4 Hilbert Spectrum Analysis | 13 |
| 2.5 Examples of HHT Spectra..... | 14 |
| 2.6 Summary | 15 |
| Chapter 3: Filed Programmable Gate Array and Nios II Soft Core Processor | 16 |
| 3.1 Filed Programmable Gate Array (FPGA) | 16 |
| 3.2 Nios II Soft Core Processor..... | 17 |
| 3.3 Summary | 20 |
| Chapter 4: Implementation of HHT | 22 |
| 4.1Uncertain Computational Consumption of EMD Sifting for Various Kinds of Signles | 22 |
| 4.2 Software Design Flow Chart of HHT | 25 |
| 4.2.1 Flow Chart of Implementation of EMD | 25 |
| 4.2.2 Software Profiling Results of EMD | 26 |
| 4.2.3 Flow Chart of HSA..... | 27 |
| 4.3 Fast Instantaneous Frequency Analyzer Based on HHT..... | 27 |
| 4.3.1 System Architecture | 28 |

| | |
|---|----|
| 4.3.2 Hardware Architecture | 30 |
| 4.3.3 Hardware Performance | 32 |
| 4.3.3 VGA Display | 34 |
| 4.4 Summary | 34 |
| Chapter 5: Hardware Acceleration of EMD | 36 |
| 5.1 Cubic Spline Interpolation..... | 36 |
| 5.2 Fixed Point System | 38 |
| 5.3 Hardware Architecture | 41 |
| 5.4 Evaluation Results | 42 |
| 5.5 Summary | 44 |
| Chapter 6: Conclusion and Future Work | 45 |
| Bibliography..... | 46 |

LIST OF FIGURES

| <i>Number</i> | <i>Page</i> |
|--|-------------|
| Figure 2.1 Flow chart of EMD..... | 6 |
| Figure 2.2 Test data | 10 |
| Figure 2.3 The original data (blue) and envelopes (green) defined by local maxima and minima, respectively, and the mean value (red) of the upper and lower envelopes..... | 11 |
| Figure 2.4 The data (red) and h1 (blue)..... | 11 |
| Figure 2.5 Repeated sifting steps with h1 and m2 | 12 |
| Figure 2.6 Repeated sifting steps with h2 and m3 | 12 |
| Figure 2.7 The first IMF | 13 |
| Figure 2.8 HHT spectrum of a frequency modulated signal..... | 14 |
| Figure 2.9 HHT spectrum of an ECG signal..... | 15 |
| Figure 3.1 Architecture of FPGAs | 16 |
| Figure 3.2 Normal LE module | 17 |
| Figure 3.3 Block diagram of Nios II processor core | 18 |
| Figure 3.4 Nios II memory and I/O architecture..... | 20 |
| Figure 4.1 Mixed chirp signal and ECG signal..... | 22 |
| Figure 4.2 IMFs from mixed chirp signal and original signal | 23 |
| Figure 4.3 Software flow chart of EMD | 26 |
| Figure 4.4 Software flow chart of HSA..... | 28 |
| Figure 4.5 System architecture of fast instantaneous frequency analyzer based on HHT..... | 29 |
| Figure 4.6 Hardware architecture of system..... | 30 |
| Figure 4.7 Hardware and software corporate architecture..... | 31 |
| Figure 4.8 Architecture FFT intellectual property core..... | 32 |
| Figure 4.8 Hardware and software corporate architecture of HSA..... | 33 |
| Figure 4.10 VGA control module..... | 34 |

| | |
|---|----|
| Figure 5.3.1 System design architecture | 41 |
| Figure 5.3.2 System design architecture with hardware accelerator | 42 |

LIST OF TABLES

| <i>Number</i> | <i>Page</i> |
|--|-------------|
| Table 4.1 Comparison of iteration times of IMFs between mixed chirp signal and ECG signal..... | 24 |
| Table 4.1 Performance of software implementation of EMD..... | 27 |
| Table 5.1 Comparison of floating point and fixed point calculation..... | 40 |
| Table 5.2 Hardware resources usage | 43 |
| Table 5.3 Comparison of software only and hardware acceleration implementation | 43 |

LIST OF ABBREVIATIONS

- ADC.** Analog to Digital Convertor
- ALU.** Arithmetic Logic Unit
- BCI.** Brain Computer Interface
- CLB.** Configurable Logic Block
- DAC.** Digital to Analog Convertor
- DSP.** Digital Signal Processor
- ECG.** Electrocardiogram
- EEG.** Electroencephalogram
- EMD.** Empirical Mode Decomposition
- FA .** Full Adder
- FFT.** Fast Fourier Transform
- FPGA.** Filed Programmable Gate Array
- GSFC.** Goddard Space Flight Center
- HDL.** Hardware Description Language
- HHT.** Hilbert-Huang Transform
- HHT-DPS.** HHT Data Processing System
- HSA.** Hilbert Spectral Analysis
- IA.** Instantaneous Amplitude
- IF.** Instantaneous Frequency
- IFFT.** Inverse Fast Fourier Transform
- IMF.** Intrinsic Mode Functions
- LAB.** Logic Array Block
- LE.** Logic Elements

LUT. Look-up Tables

MMU. Memory Management Unit

MPU. Memory Protection Unit

NASA. National Aeronautics and Space Administration

PC. Personal Computer

PPG. Photoplethysmogram

PTT. Pulse Transit Time

SDRAM. Synchronous Dynamic Random Access Memory

SOPC. System On Programmable Chip

SRAM. Static Random Access Memory

ACKNOWLEDGMENTS

I am grateful to the many people who have given me the possibilities to complete this research and thesis.

First of all, I must express my special thanks to my supervisors Prof. Vai Mang I and Dr. Mak Peng Un, not only for their valuable guidance, support and comments to my research work and university life, but also introducing me to this wonderful biomedical engineering and digital signal processing world. Without them, I never know anything about this field.

My appreciation also to all of my teachers in Biomedical Engineering Joint-Research Group including Dr. Chao Sam, Dr. Mak Pui In, Dr. Wan Feng and Dr. Wong Fai, for both of their guidance in regular meetings and the support in university life. And I am deeply indebted to Dr. Mak Pui In for participating in my defense committee. I have to thank my BME lab-mates and classmates including but not limited to Mr. Jeong Chao In, Mr. Chan Chang Hao, Mr. Zhang Tan Tan, Mr. Mou Pedro, Mr. Pun Sio Hang, for taking care of me these days.

Last but not the least, I sincerely thank my family. Without their unlimited love and support, everything is impossible.