A Novel Readout Front-End Circuit Topology for Flexible Biopotential Signal Acquisition System

一種適用于靈活采集生物電信號的新型前端電路結構

by

LI, JINTAO

Master of Science in Electrical and Electronics Engineering

2009

Faculty of Science and Technology
University of Macau

A Novel Readout Front-End Circuit Topology for Flexible Biopotential Signal Acquisition System

by

LI, JINTAO

A thesis submitted in partial fulfillment of the requirements for the degree of

Master of Science in Electrical and Electronics Engineering

Faculty of Science and Technology
University of Macau

2009

Approved by _____
Supervisor

_____

_____

_____

Date _____

In presenting this thesis in partial fulfillment of the requirements for a Master's degree at the University of Macau, I agree that the Library and the Faculty of Science and Technology shall make its copies freely available for inspection. However, reproduction of this thesis for any purposes or by any means shall not be allowed without my written permission. Authorization is sought by contacting the author at

Address: Biomedical Engineering Laboratory, NG05-06, Choi Kai Yau Building, University of Macau, Av. Padre Tomás Pereira S.J., Taipa, Macau SAR, P. R. China.

Telephone: (+853) 83974276
Fax: (+853) 83974276
E-mail: jingtao@eee.umac.mo

Signature _____

Date _____

University of Macau

Abstract

A NOVEL READOUT FRONT-END CIRCUIT TOPOLOGY FOR FLEXIBLE BIOPOTENTIAL SIGNAL ACQUISITION SYSTEM

by LI, JINTAO

Thesis Supervisor: Prof. Vai, Mang I
Thesis Co-Supervisor: Dr. Mak, Peng Un
Master of Science in Electrical and Electronics Engineering

Information of extracted biopotential signals such as ECG, EEG and EMG is widely used for medical treatment purpose and health care applications. There is an increasing demand for flexible/portable biopotential signal acquisition systems which can be not only applied for long time medical monitoring, but also extended to home health care, sports and entertainment applications. The key to this kind of systems is the analog readout front-end. The analog readout front-end extracts the biosignals directly from human body and defines the extracted signal quality.

The most critical and power consuming building block of the readout front-end circuit is the biopotential amplifier. Biopotential amplifier emerges several design challenges due to the complex environment of human body and different applications. In general, biopotential amplifier should have high CMRR to reject strong common mode interference from mains and low noise in order to acquire the extremely weak signals.

This thesis proposes a novel flexible analog readout front-end circuit topology oriented to flexible and portable biopotential signal acquisition systems. The essential contribution of this work is the new chopped current mode instrumentation amplifier (CMIA) based on second generation current conveyor while involving power supply current sensing technique. The new CMIA gains very low noise performance by using chopper modulation technique. At the same time, high CMRR, low power consumption and other advantages are achieved by the aid of the current mode topology and current sensing technique realized by the new designed low transconductance current mirrors.

Two complete analog readout front-ends are implemented and simulated using the proposed chopped CMIA with two advanced low pass filters (LPFs): general purpose readout front-end using 100-Hz 5^{th}-order G_m-C LPF and portable EEG readout front-end using 40-Hz source-follower-based LPF. The simulation results show that the designed circuits meet the basic requirements of the long time portable biopotential acquisition application and are ready for connecting to next stages, e.g. ADC and DSP.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS AND SYMBOLS

Abbreviations

ADC Analog to Digital Convertor

CBIA Current Balancing Instrumentation Amplifier

CCII Second Generation Current Conveyor

CMIA Current Mode Instrumentation Amplifier

CMRR Common Mode Rejection Ratio

DR Dynamic Range

DSP Digital Signal Processor

ECG Electrocardiogram

EEG Electroencephalogram

EMG Electromyogram

GBW Gain Bandwidth Product

Gm-C LPF Transconductance-Capacitor Low Pass Filter

HPF High Pass Filter

IA Instrumentation Amplifier

LPF Low Pass Filter

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NMOS N-Channel Metal Oxide Semiconductor

NSF NMOS Source Follower

OTA Operational Transconductance Amplifier

PMOS P-Channel Metal Oxide Semiconductor

PSD Power Spectral Density

SCIA Switched-capacitor Instrumentation Amplifier

SFB LPF Source Follower Based Low Pass Filter

THD Total Harmonic Distortion

Symbols

$\mathbf{A_c}$ Common mode gain of op amp

$\mathbf{A_d}$ Differential mode gain of op amp

$\mathbf{f_{3dB}}$ 3 dB low cutoff frequency of amplifier

$\mathbf{f_c}$ Conner frequency of amplifier

$\mathbf{f_{c,\ 1/f}}$ Conner frequency of 1/f noise

$\mathbf{f_{chop}}$ Chopping frequency of chopper

$\mathbf{f_{cutoff}}$ Low cutoff frequency of LPF

$\mathbf{G_c}$ Common mode gain

$\mathbf{G_d}$ Differential mode gain

$\mathbf{G_{cc}}$ Common mode gain to common mode input only

$\mathbf{G_{cd}}$ Common mode gain to differential mode input only

$\mathbf{G_{dc}}$ Differential mode gain to common mode input only

$\mathbf{G_{dd}}$ Differential mode gain to differential mode input only

$\mathbf{g_m}$ Transconductance of MOSFET

$\mathbf{I_D}$ Drain current of a transistor

n Operating value of substrate factor of the number 1.5

$\mathbf{R_{on,\ eq}}$ Equivalent resistance of CMOS complementary switch

$\mathbf{S_0}$ Thermal noise level of an amplifier

$\mathbf{S_{in}}$ Double-sided input referred noise power spectral density of amplifier

$\mathbf{S_{in,\ 1/f}}$ 1/f noise component of S_{in}

$\mathbf{S_{in,\ thermal}}$ Thermal noise component of S_{in}

$\mathbf{U_T}$ Thermal voltage at room temperature

$\mathbf{V_{Clk}}$ Chopping clock voltage

$\mathbf{V_{hc}}$ Half-cell potential

$\mathbf{v_n}$ Output Noise Voltage of Amplifier

$\mathbf{v_{off}}$ Offset Voltage of Amplifier

$\mathbf{V_{THN}}$ Threshold voltage of NMOS transistor

$\mathbf{V_{THP}}$ Threshold voltage of PMOS transistor

ACKNOWLEDGMENTS

I would like to express my sincere gratitude to all the people who help me to make these words realized.

First of all, I must express my special thanks to my supervisors Prof. Mang I Vai and Dr. Peng Un Mak, not only for their valuable guidance, support and comments to my research work and university life, but also introducing me to this wonderful biomedical engineering and microelectronics circuit world. Without them, I never know anything about this field.

I would like to thank Dr. Pui In Mak from Analog and Mixed Signal VLSI Laboratory, for his professional discussions on circuit design issues. I learn much from him. I would like to thank my B.Sc supervisor Prof. Ming Chui Dong. He is the first person who leads me to engineering research work.

I have to thank Mr. Tan Tan Zhang and Mr. Chang Hao Chen from Biomedical Engineering Laboratory, for their valuable support to this thesis work. Mr. Zhang has done many simulation works to help me organizing and analyzing the results. I also would like to express my thanks to Mr. Sio Hang Pun for his help and comments on my work, and Mr. Pedro A. Mou, he helps me a lot for computer issues.

I am grateful to University of Macau and Biomedical Engineering Laboratory. Both of them provide me the chance to be an electronics engineering student and the good environment for conducting my M.Sc degree study. I am grateful to all the friends there for the fun we had all those years.

Last but not the least, I sincerely thank my parents. Without their unlimited love and support, everything is impossible. Words are not enough for my girl friend, Qian Hua Zheng, she always believes and supports me even I am far away from her for more than seven years.