

**Low Power High Efficiency Excess-Loop-Delay  
Compensation Techniques in Continuous-Time  
Delta-Sigma Modulators**

by

**Cai Chen-Yan, Joy**

**(M-A9-6522-2)**



**Faculty of Science and Technology  
University of Macau**

**Low Power High Efficiency Excess-Loop-Delay  
Compensation Technique in Continuous-Time Delta-Sigma  
Modulators**

by

**Cai Chen-Yan, Joy**

A thesis submitted in partial fulfillment of the  
requirements for the degree of

Master of Science  
in  
Electrical and Electronic Engineering

Faculty of Science and Technology  
University of Macau

2013

澳門大學

Approved by \_\_\_\_\_  
Supervisor

\_\_\_\_\_  
Co-Supervisor

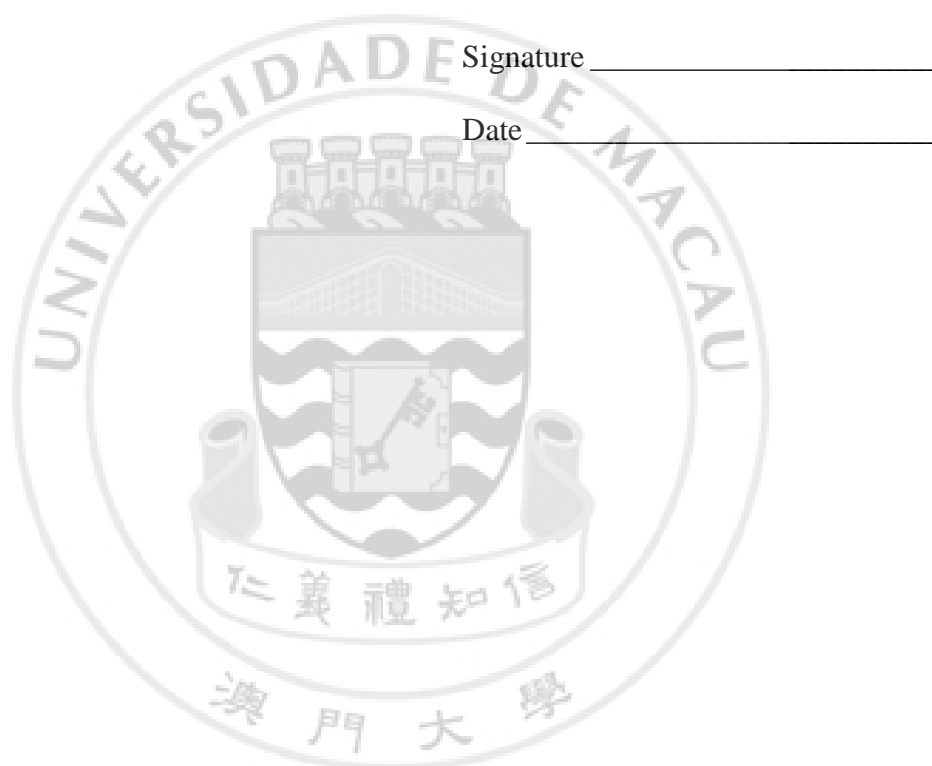
\_\_\_\_\_

Date \_\_\_\_\_

In presenting this thesis in partial fulfillment of the requirements for a Master's degree at the University of Macau, I agree that the Library and the Faculty of Science and Technology shall make its copies freely available for inspection. However, reproduction of this thesis for any purposes or by any means shall not be allowed without my written permission. Authorization is sought by contacting the author at

Address: State Key Laboratory of Analog and Mixed-Signal VLSI, FST,  
University of Macau, Av. Padre Tom ás Pereira, Taipa, Macao, China.

E-mail: chenyan.cai@gmail.com



## ABSTRACT

Because of the convenient and powerful function of mobile telecommunication devices, the demand of it is tremendously increased in the whole world wide nowadays. As the connection element between the analog and digital signal world, the modulators are obligatory. On account of the merits of low power consumption, small silicon area, large signal bandwidth, and also inherent anti-aliasing function, the Continuous-Time (CT)  $\Sigma\Delta$  modulator has been extensively used in wideband telecommunication systems.

However, the performance of CT  $\Sigma\Delta$  modulators is restricted by the non-idealities of practical circuit elements. Excess Loop Delay (ELD) is one of the dominant effects induces the error in the Transfer Function, and then reduces the performance of the CT  $\Sigma\Delta$  modulator. Even worse, the error may cause the instability of the modulator.

This thesis proposes three different techniques with the properties of low-power and high-efficiency to compensate the ELD effect of CT  $\Sigma\Delta$  modulators. The first technique is based on the Gm-C loop filter and with one passive resistor added. After verifying it in 65nm CMOS technique, the proposed technique can reduce the power consumption up to 32% and compensate up to half of clock cycle delay amount. The second technique employs digital logic elements and an RC feedback network for the active-RC loop filter to track the amount of ELD up to half of clock cycle synchronously on a real-time modulator, and then compensate it. It is verified in 65nm CMOS process, compare with the traditional technique, power reduced from 6.5mW to 5.45mw. And the third technique is for hybrid active-passive integrators. The efficiency of the proposed compensation techniques are implemented in the designed modulators and verified by the transistor-level simulation as well. This technique can compensate the delay amount up to one clock cycle and reduced more than half of power dissipation. Compare with the traditional techniques, these three techniques are quite low power dissipation and can compensate the ELD effect effectively.

## KEY WORDS

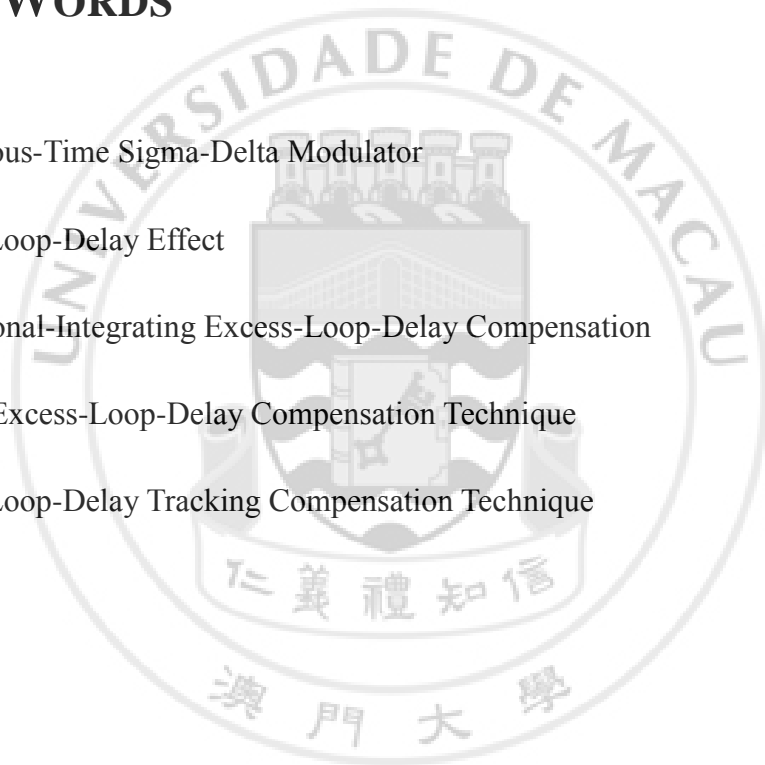
Continuous-Time Sigma-Delta Modulator

Excess-Loop-Delay Effect

Proportional-Integrating Excess-Loop-Delay Compensation

Passive Excess-Loop-Delay Compensation Technique

Excess-Loop-Delay Tracking Compensation Technique



## ACKNOWLEDGEMENT

I wish to express my gratitude to my Supervisors Doc. Sin Sai Weng and Prof. U Seng-Pan for their supports and guidance during the course of my M.Sc. Study at University of Macau. I would also like to thank them for leading me into this one of the most challenge and worthwhile design integrated circuit areas in the electronic world. Few arduous problems can be solved without their immensely patient and guidance.

Particularly, I would like to thank to Mr. Tim Jiang for his valuable suggestions on my research work, as well as developing new ideas; and also Mr. Clark Chen for the pleasant and helpful cooperation with him.

Besides, the lab mates such as Alpha Zhao, Ray Wang, Arshad, Steve Ding, Steven Wu, Hugh Du, Gavin Zhang, Dick Wong, Guo He, Jankey Zhong, Julia Zhu and Ivor Chan gave me lots of assistances during the project. I appreciate their friendship as well as help very much. I also want to thank Leo Ng and Lewis Lei for their lab equipment support.

I would like to thank the Research Committee of University of Macau and Macau Science and Technology Development Fund (FDCT) for the finical support during my graduate study.

Last, I express my deepest gratitude to my family for their loves, kindness encouragement and support. Finally, I express sincerely my gratitude once more to all of the people who have contributed to this work.



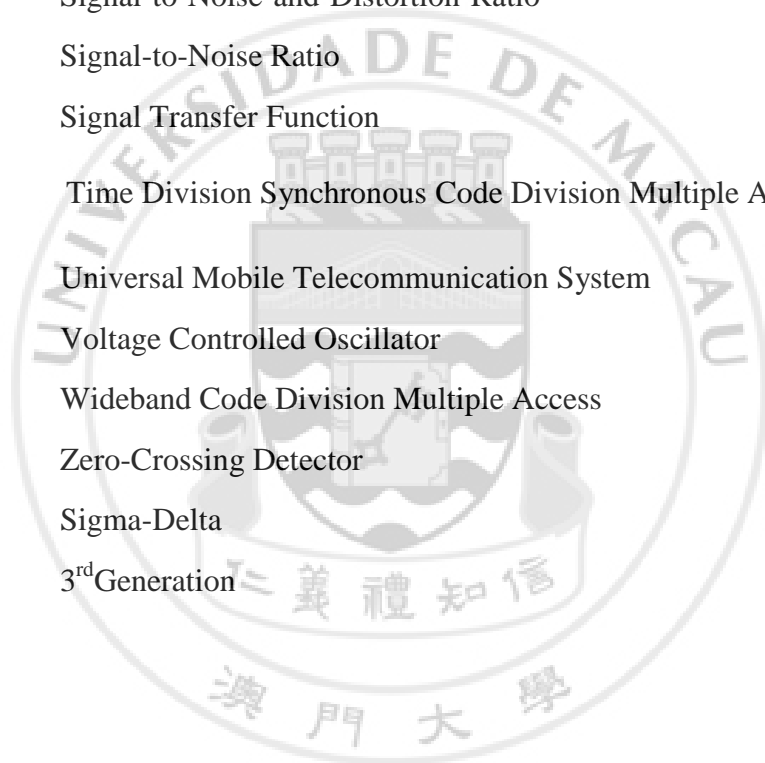
*To my family*

## LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
AMS	Analog Mixed-Signal
AP	Active-Passive
CC	Compensation Component
CIFB	Chain of Integrators with distributed FeedBack
CIFF	Chain of Integrators with weighted Feed-Forward
CLG	Control Logic Generator
CT	Continuous-Time
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DFF	D-Flip-Flop
DSP	Digital Signal Processor
DT	Discrete-Time
DWA	Data Weighted Averaging
ELD	Excess-Loop Delay
GSM	Global System for Mobile
HRZ	Half-Return-to-Zero
HSPA	High Speed Packet Access
IIT	Impulse Invariant Transform
IBN	In-Band-Noise
MASH	Multi-stage noise Shaping
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OSR	OverSampling Ratio
Op-Amp	Operational Amplifier
PA	Power Amplifier



PLL	Phase Lock Loop
PM	Power Management
PP	Pulse-Position
PS	Pulse Shape
PSD	Power Spectral Density
PW	Pulse-Width
RZ	Return-to-Zero
SNDR	Signal-to-Noise-and-Distortion-Ratio
SNR	Signal-to-Noise Ratio
STF	Signal Transfer Function
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
UMTS	Universal Mobile Telecommunication System
VCO	Voltage Controlled Oscillator
WCDMA	Wideband Code Division Multiple Access
ZCD	Zero-Crossing Detector
$\Sigma\Delta$	Sigma-Delta
3G	3 <sup>rd</sup> Generation



## TABLE OF CONTENTS

ABSTRACT .....	III
KEY WORDS .....	IV
ACKNOWLEDGEMENT .....	V
LIST OF ABBREVIATIONS .....	VII
TABLE OF CONTENTS .....	IX
LIST OF FIGURES .....	XII
LIST OF TABLES .....	XVI
CHAPTER 1 INTRODUCTION .....	1
1.1 BACKGROUND AND APPLICATION .....	1
1.1.1 3G WIRELESS COMMUNICATIONS .....	1
1.1.2 APPLICATION OF ADCs IN 3G WCDMA RECEIVER .....	5
1.2 RESEARCH MOTIVATION.....	7
1.3 THESIS ORGANIZATION.....	9
1.4 STATEMENT OF ORIGINALITY .....	11
CHAPTER 2 ELEMENTARY OF $\Delta\Sigma$ MODULATION .....	13
2.1 INTRODUCTION.....	13
2.2 QUANTIZATION AND OVERSAMPLING .....	13
2.3 $\Delta\Sigma$ MODULATION.....	18
2.4 SECOND AND HIGHER ORDER MODULATION .....	22
2.5 SINGLE-STAGE AND MULTI-STAGE $\Delta\Sigma$ TOPOLOGY.....	25
2.5.1 SINGLE-STAGE MODULATOR.....	25
2.5.2 MULTI-STAGE MODULATION .....	27
2.6 SUMMARY.....	29
CHAPTER 3 CONTINUOUS-TIME (CT) $\Delta\Sigma$ MODULATION.....	31
3.1 INTRODUCTION.....	31
3.2 ADVANTAGES OF CT $\Delta\Sigma$ MODULATION.....	31
3.3 CONVERSION OF A DT $\Delta\Sigma$ MODULATION.....	32
3.3.1 IMPULSE-INVARIANT TRANSFORM .....	33
3.3.2 MODIFIED Z-TRANSFORM.....	35

3.4	IMPLICIT ANTI-ALIASING FILTERING .....	38
3.5	ALTERNATIVES FOR CT FILTER IMPLEMENTATION .....	41
3.5.1	ACTIVE RC INTEGRATOR.....	41
3.5.2	Gm-C INTEGRATOR.....	43
3.5.3	PASSIVE RC INTEGRATOR.....	44
3.6	NON-IDEALITY ISSUES OF PRACTICAL CT $\Delta\Sigma$ MODULATOR.....	46
3.6.1	TIME CONSTANT VARIATION.....	46
3.6.2	FINITE GAIN AND GBW FOR THE OP-AMP IN CT INTEGRATOR.....	48
3.6.3	CLOCK JITTER EFFECT .....	50
3.7	SUMMARY.....	53
CHAPTER 4 EXCESS-LOOP-DELAY (ELD) AND ITS COMPENSATION		
TECHNIQUES OF CT $\Delta\Sigma$ MODULATORS WITH ACTIVE RC		
INTEGRATOR.....		
4.1	INTRODUCTION .....	54
4.2	ELD EFFECT IN CT $\Delta\Sigma$ MODULATOR.....	54
4.2.1	DELAY AFFECTS THE RETURN-TO-ZERO (RZ) FEEDBACK.....	55
4.2.2	DELAY AFFECTS THE NON-RETURN-TO-ZERO (NRZ) FEEDBACK....	58
4.3	EXISTED ELD COMPENSATION METHODS .....	61
4.3.1	TRADITIONAL COMPENSATION TECHNIQUE WITH ADDITIONAL	
	FEEDBACK PATH .....	62
4.3.2	ELD COMPENSATION METHOD WITH A DIGITAL DIFFERENTIATOR .	64
4.3.3	ELD COMPENSATION WITH PI-ELEMENT .....	65
4.4	SUMMARY.....	68
CHAPTER 5 AN ELD TRACKING COMPENSATION TECHNIQUE FOR		
ACTIVE-RC CT $\Sigma\Delta$ MODULATORS .....		
5.1	INTRODUCTION.....	69
5.2	ELD TRACKING COMPENSATION METHOD.....	70
5.2.1	WORKING PRINCIPLE OF COMPENSATION COMPONENT .....	72
5.2.2	DELAY ISSUES OF COMPENSATION COMPONENT.....	75
5.3	DESIGN EXAMPLE AND SIMULATION VERIFICATION .....	77
5.4	SUMMARY.....	81

CHAPTER 6	A PASSIVE ELD COMPENSATION TECHNIQUE FOR GM-C BASED CT $\Delta\Sigma$ MODULATORS.....	82
6.1	INTRODUCTION.....	82
6.2	PROPOSED TECHNIQUE WITH GM-C INTEGRATOR.....	83
6.3	DESIGN EXAMPLE OF CT $\Delta\Sigma$ MODULATOR.....	88
6.4	SIMULATION VERIFICATION.....	89
6.5	SUMMARY.....	92
CHAPTER 7	AN ELD COMPENSATION TECHNIQUE FOR CT $\Delta\Sigma$ MODULATORS WITH HYBRID ACTIVE-PASSIVE (AP) LOOP- FILTERS.....	93
7.1	INTRODUCTION.....	93
7.2	LOOP FUNCTION OPTIMIZATION WITH SINGLE-BIT QUANTIZER FOR HYBRID AP CT $\Delta\Sigma$ MODULATOR.....	95
7.3	ELD COMPENSATION FOR A CT $\Delta\Sigma$ MODULATOR WITH HYBRID ACTIVE- PASSIVE LOOP-FILTERS.....	100
7.3.1	ELD EFFECT IN THE HYBRID AP CT $\Delta\Sigma$ MODULATOR.....	101
7.3.2	TRADITIONAL ELD COMPENSATION METHOD.....	104
7.3.3	SIMPLE RESISTOR ADDER METHOD.....	105
7.3.4	PASSIVE ELD COMPENSATION TECHNIQUE FOR HYBRID ACTIVE- PASSIVE INTEGRATORS.....	107
7.4	DESIGN EXAMPLE OF HYBRID AP CT $\Delta\Sigma$ MODULATOR.....	109
7.5	SUMMARY.....	114
CHAPTER 8	CONCLUSION.....	115
8.1	SUMMARY OF THE THESIS.....	115
8.2	CONCLUSION OF THE THESIS.....	118
8.3	THE FUTURE WORK.....	119
	BIBLIOGRAPHY.....	120

## LIST OF FIGURES

Fig.1.1 Estimation of wireless communication technology.....	2
Fig.1.2 Function of the 3G mobile phone.....	3
Fig.1.3 The investigation of mobile infrastructure in the worldwide.....	4
Fig.1.4 Worldwide mobile broadband service revenue forecasting.....	5
Fig.1.5 The circuit functions of a typical mobile communication system.....	6
Fig.1.6 The application range of over-sampling Sigma Delta and Pipeline ADC.....	7
Fig.2.1 Transfer curve (a) and the quantization error of a uniform multi-level quantizer (b).....	14
Fig.2.2 Quantization noise distribution in both Nyquist rate and oversampling quantization.....	17
Fig.2.3 Basic architecture (a) and the corresponding linear model for the $\Sigma\Delta$ modulator (b).....	18
Fig.2.4 Linear model for a 1 <sup>st</sup> order $\Sigma\Delta$ modulator employing DT integrator.....	19
Fig.2.5 The PSDs for the quantization noise from an oversampling quantizer and a $\Sigma\Delta$ modulator.....	21
Fig.2.6 A second order $\Sigma\Delta$ modulator.....	22
Fig.2.7 The $M$ th order $\Sigma\Delta$ modulator.....	24
Fig.2.8 Structures of a 5 <sup>th</sup> order (a) CIFB $\Sigma\Delta$ modulator and (b) CIFF $\Sigma\Delta$ modulator. .....	26
Fig.2.9 2-1 MASH $\Sigma\Delta$ modulator.....	28
Fig.3.1 Block diagrams for (a) DT and (b) CT $\Sigma\Delta$ modulator.....	33
Fig.3.2 The feedback loop filters of (a) DT and (b) CT $\Delta\Sigma$ modulator.....	34
Fig.3.3 The HRZ feedback waveform.....	36
Fig.3.4 A modified representation for CT $\Sigma\Delta$ modulator.....	39
Fig.3.5 A representation for the $\Sigma\Delta$ modulator with CT input transfer function.....	39
Fig.3.6 CT $\Sigma\Delta$ modulator with input anti-aliasing filtering.....	40
Fig.3.7 STF of a 2 <sup>nd</sup> order CT $\Delta\Sigma$ modulator.....	41
Fig.3.8 Structure of active RC integrator.....	42
Fig.3.9 Transformation block of active RC integrator.....	42

Fig.3.10 The Gm-C integrator structure. ....	43
Fig.3.11 Structure of the passive RC filter. ....	44
Fig.3.12 Transformation block of passive RC integrator. ....	45
Fig.3.13 System architecture of hybrid AP CT $\Delta\Sigma$ modulator. ....	45
Fig.3.14 A 2 <sup>nd</sup> order CT $\Delta\Sigma$ Modulator with active RC integrators and one-bit quantizer.....	47
Fig.3.15 System sensitivity to the coefficient $k_1$ variation.....	47
Fig.3.16 System sensitivity to the coefficient $k_2$ variation.....	48
Fig.3.17 Equivalent small signal model of single-input single-output active RC integrator. ....	49
Fig.3.18 Clock-jitter induced (a) PW variation and (b) PP variation .....	52
Fig.4.1 Rectangular waveforms of: (a) RZ feedback, (b) NRZ feedback.....	55
Fig.4.2 RZ feedback waveform with ELD $\tau_d$ .....	56
Fig.4.3 System architectures of a 2 <sup>nd</sup> order (a) discrete-time and (b) active continuous- time $\Delta\Sigma$ modulator. ....	56
Fig.4.4 NTF pole-zero locations of RZ feedback with delay $\tau_d$ . ....	57
Fig.4.5 The NTF for RZ feedback with different values of delay $\tau_d$ .....	58
Fig.4.6 NRZ feedback pulse due to delay $\tau_d$ .....	59
Fig.4.7 Pole and zero locations of NRZ feedback when there is delay $\tau_d$ .....	60
Fig.4.8 The NTF with different value of delay $\tau_d$ with NRZ feedback .....	61
Fig.4.9 Traditional ELD compensation method. ....	63
Fig.4.10 ELD compensation with a digital differentiator. ....	64
Fig.4.11 The PI-element ELD compensation method. ....	66
Fig.4.12 Realization of a PI-element for ELD compensation for an active RC integrator .....	67
Fig.5.1 NRZ DAC pulse with: a) ideal case, b) with a certain amount of delay $\tau_d$ .....	70
Fig.5.2 Waveform of the proposed compensation technique. ....	71
Fig.5.3 Block diagram of the proposed ELD tracking compensation technique .....	72
Fig.5.4 Clock and reset signals for Compensation Component (CC).....	73
Fig.5.5 Implementation of the Control Logic Generator (CLG) with digital logic. ....	73
Fig.5.6 Illustration of the proposed ELD tracking compensation technique. ....	74
Fig.5.7 Waveforms of a) CLK0 b) theoretical $V_{Cc}$ c) $V_{Cc}$ with delay considered.....	76

Fig.5.8 Current IA of the RC feedback network for different values of the time constant $\tau$ .....	77
Fig.5.9 Settle error tolerance of the RC feedback network.....	78
Fig.5.10 Comparison of simulation results for 2 different cases when there is 50% $T_s$ delay in the quantizer. ....	79
Fig.5.11 Simulation results for system sensitivity to ELD in a 2nd order CT $\Sigma\Delta$ modulator with or without the proposed compensation technique. ....	80
Fig.6.1 An ideal 2nd order CT $\Sigma\Delta$ modulator with CIFB topology. ....	83
Fig.6.2 Fully differential Gm-C loop filter with CMFB.....	84
Fig.6.3 Basic concept for ELD compensation with PI-element using Gm-C integrator .....	85
Fig.6.4 Proposed ELD compensation with PI-element using Gm-C integrator with passive implementation.....	86
Fig.6.5 Proposed PI-element ELD compensation with parasitic capacitor $C_p$ .....	87
Fig.6.6 Modified improved ELD compensation with PI-element using Gm-C integrator structure.....	87
Fig.6.7 Traditional ELD compensation with Gm-C integrator in CT $\Sigma\Delta$ modulator. .	88
Fig.6.8 Circuit schematic of the proposed ELD compensation structure with Gm-C integrator in a 2nd order, 1-bit, CT sigma-delta modulator with NRZ DAC.88	
Fig.6.9 Comparison of simulation results for 2 different cases when there is 50% $T_s$ delay in the quantizer .....	90
Fig.6.10 Simulation results for system sensitive to ELD in a 2nd order CT $\Sigma\Delta$ modulator with proposed compensation technique and without compensation .....	91
Fig.7.1 System architecture of hybrid AP CT $\Delta\Sigma$ modulator. ....	96
Fig.7.2 NTF pole-zero locations for the 2 <sup>nd</sup> order active CT $\Delta\Sigma$ modulator and the hybrid AP modulator without optimization. ....	97
Fig.7.3 Calculated NTF for the un-optimized hybrid AP and the active CT $\Delta\Sigma$ modulator .....	97
Fig.7.4 Analytical model for loop function optimization of AP CT $\Delta\Sigma$ modulator ....	98

Fig.7.5 Calculated NTFs for the hybrid AP CT $\Delta\Sigma$ modulator with different passive loop filter gain scaling values. ....	99
Fig.7.6 NTF pole-zero location variation for the AP CT $\Delta\Sigma$ modulator with the passive loop filter gain scaling from 1 to 0.....	100
Fig.7.7 NRZ DAC feedback pulse: a) Ideal case, b) With delayed $\tau_d$ . ....	102
Fig.7.8 The NTF when the hybrid AP modulator contains and does not contains one clock cycle delay effect with $a=0.25$ . ....	103
Fig.7.9 Traditional ELD compensation method for a 2 <sup>nd</sup> order CT $\Delta\Sigma$ modulator with hybrid AP integrators. ....	104
Fig.7.10 The ideal NTF (without ELD effect), the NTF for the modulator contains one clock cycle delay effect and the NTF with delay after traditional compensation with $a=0.25$ . ....	105
Fig.7.11 Passive analog adder current feedback in (a) active and (b) passive loop-filters. ....	106
Fig.7.12 The model of the passive technique to compensate the ELD effect in the hybrid AP modulator.....	107
Fig.7.13 Circuit implementation of the passive ELD compensation technique for a passive RC integrator.....	108
Fig.7.14 Passive ELD compensation technique with hybrid AP integrators. ....	108
Fig.7.15 Circuit schematic of the passive ELD compensation structure in a 2 <sup>nd</sup> order, 1-bit, CT $\Delta\Sigma$ modulator with hybrid AP integrators and NRZ DAC.....	110
Fig.7.16 Comparison of simulation results for 2 different cases ( $Pin_{red}=-20dBFS$ , $Pin_{blue}=-2dBFS$ ) when there is 1Ts delay in the quantizer. ....	112
Fig.7.17 SNDR versus input signal amplitude. ....	112
Fig.7.18 The value of R0 vesus SNDR of the system. ....	112
Fig.7.19 Simulation results for system sensitivity to ELD in a 2 <sup>nd</sup> order Hybrid AP CT $\Delta\Sigma$ modulator with and w/o the proposed compensation technique, with $Pin_{low}=-20dBFS$ and $Pin_{high}=-2dBFS$ .....	113



## LIST OF TABLES

Table3. 1 THE CORRESPONDING LOOP FILTER ORDER WITH THE MODIFIED Z-TRANSFORM.....	37
Table5. 1 THE COMPARISON BETWEEN THIS WORK AND EXISTED ONES .....	80
Table6. 1 COMPARISON BETWEEN PROPOSED TECHNIQUE AND THE EXISTED STRUCTURES .....	91
Table7. 1 COMPARISON OF PERFORMANCE OF DIFFERENT STRUCTURES .....	113

