# Low Power High Efficiency Excess-Loop-Delay Compensation Techniques in Continuous-Time Delta-Sigma Modulators

by

**Cai Chen-Yan, Joy**

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requirements for the degree of

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Approved by _____
Supervisor

_____
Co-Supervisor

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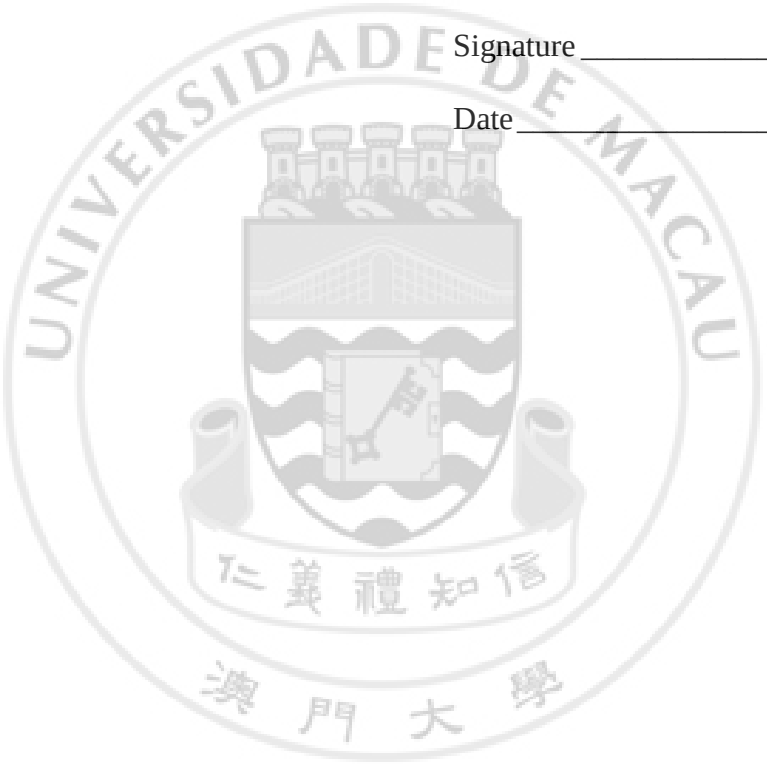
Address: State Key Laboratory of Analog and Mixed-Signal VLSI, FST, University of Macau, Av. Padre Tomás Pereira, Taipa, Macao, China.

E-mail: chenyan.cai@gmail.com

Signature _____

Date _____



# ABSTRACT

Because of the convenient and powerful function of mobile telecommunication devices, the demand of it is tremendously increased in the whole world wide nowadays. As the connection element between the analog and digital signal world, the modulators are obligatory. On account of the merits of low power consumption, small silicon area, large signal bandwidth, and also inherent anti-aliasing function, the Continuous-Time (CT) ΣΔ modulator has been extensively used in wideband telecommunication systems.

However, the performance of CT ΣΔ modulators is restricted by the non-idealities of practical circuit elements. Excess Loop Delay (ELD) is one of the dominant effects induces the error in the Transfer Function, and then reduces the performance of the CT ΣΔ modulator. Even worse, the error may cause the instability of the modulator.

This thesis proposes three different techniques with the properties of low-power and high-efficiency to compensate the ELD effect of CT ΣΔ modulators. The first technique is based on the Gm-C loop filter and with one passive resister added. After verifying it in 65nm CMOS technique, the proposed technique can reduce the power consumption up to 32% and compensate up to half of clock cycle delay amount. The second technique employs digital logic elements and an RC feedback network for the active-RC loop filter to track the amount of ELD up to half of clock cycle synchronously on a real-time modulator, and then compensate it. It is verified in 65nm CMOS process, compare with the traditional technique, power reduced from 6.5mW to 5.45mw. And the third technique is for hybrid active-passive integrators. The efficiency of the proposed compensation techniques are implemented in the designed modulators and verified by the transistor-level simulation as well. This technique can compensate the delay amount up to one clock cycle and reduced more than half of power dissipation. Compare with the traditional techniques, these three techniques are quite low power dissipation and can compensate the ELD effect effectively.

# KEY WORDS

Continuous-Time Sigma-Delta Modulator

Excess-Loop-Delay Effect

Proportional-Integrating Excess-Loop-Delay Compensation

Passive Excess-Loop-Delay Compensation Technique

Excess-Loop-Delay Tracking Compensation Technique

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***To my family***

# LIST OF ABBREVIATIONS

| | |
|---|---|
| ADC | Analog to Digital Convertor |
| AMS | Analog Mixed-Signal |
| AP | Active-Passive |
| CC | Compensation Component |
| CIFB | Chain of Integrators with distributed FeedBack |
| CIFF | Chain of Integrators with weighted Feed-Forward |
| CLG | Control Logic Generator |
| CT | Continuous-Time |
| DAC | Digital-to-Analog Converter |
| DEM | Dynamic Element Matching |
| DFF | D-Flip-Flop |
| DSP | Digital Signal Processor |
| DT | Discrete-Time |
| DWA | Data Weighted Averaging |
| ELD | Excess-Loop Delay |
| GSM | Global System for Mobile |
| HRZ | Half-Return-to-Zero |
| HSPA | High Speed Packet Access |
| IIT | Impulse Invariant Transform |
| IBN | In-Band-Noise |
| MASH | Multi-stAge noise SHaping |
| NRZ | Non-Return-to-Zero |
| NTF | Noise Transfer Function |
| OSR | OverSampling Ratio |
| Op-Amp | Operational Amplifier |
| PA | Power Amplifier |

| | |
|---|---|
| PLL | Phase Lock Loop |
| PM | Power Management |
| PP | Pulse-Position |
| PS | Pulse Shape |
| PSD | Power Spectral Density |
| PW | Pulse-Width |
| RZ | Return-to-Zero |
| SNDR | Signal-to-Noise-and-Distortion-Ratio |
| SNR | Signal-to-Noise Ratio |
| STF | Signal Transfer Function |
| TD-SCDMA | Time Division Synchronous Code Division Multiple Access |
| UMTS | Universal Mobile Telecommunication System |
| VCO | Voltage Controlled Oscillator |
| WCDMA | Wideband Code Division Multiple Access |
| ZCD | Zero-Crossing Detector |
| ΣΔ | Sigma-Delta |
| 3G | 3rd Generation |

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