Abstract

INTEGRATION of high-frequency analog filtering into the system Analog Front-End (AFE) is increasingly demanded for the ever growing high-speed communications and signal processing solutions with the corresponding advances in Integrated Circuit (IC) technology. Although the AFEs represent a small portion of the total mixed-signal system chip, they usually are the speed and performance bottleneck of the system. Especially, the design of the AFEs becomes more and more challenging due to the continuous lowering of the supply and increasing of the operation speed, as well as noisying of the working environment driven by the constant growing digital signal processing (DSP) core.

This work presents a multirate sampled-data interpolation technique and its Switched-Capacitor (SC) implementation for very high frequency filtering (over hundreds of MHz) while having also dual inherent advantages of reducing the speed of the digital-to-analog converter and the DSP core together with the simplification of the post continuous-time smoothing filter.

The first part of this work proposes different novel SC multirate polyphase-based interpolation architectures, which efficiently eliminate the traditional sample-and-hold shaping effects at lower input rate, with the optimization in the circuit sensitivity, speed requirement and component count of the active elements. Physical IC technology imperfections related with IC implementation are also investigated thoroughly; and the advanced circuit techniques including gain, offset and mismatch calibrations are also proposed and analyzed to tackle such limitations.

The second part focuses on the tailor-made optimum design and implementation in 0.35 μm CMOS of two SC interpolating filters: one for the baseband and another for the frequency-translated mode operation. The first one implements a 3-stage 8-fold SC interpolating filter with 5.5 MHz bandwidth and 108 MHz output sampling rate for a NTSC/PAL CCIR 601 digital video at 3 V supply. Another prototype chip is a 2.5 V, 15-tap, 57 MHz SC FIR bandpass interpolating filter with 4-fold frequency up-translation for 22-24 MHz inputs at 80 MHz to 56-58 MHz outputs at 320MHz using in a Direct-Digital Frequency Synthesis (DDFS) system for wireless communication. Its experimental results match splendidly with theoretical expectations and validate the effectiveness of the presented architectural-, circuit- and layout-level optimization schemes wrestling with different design challenges at such high-frequency operation. This prototype filter chip works up to 400 MHz with still satisfactory performance, and has so far the highest operating frequency, highest filter order and highest center frequency with highest dynamic range under the lowest supply voltage when compared to the previously reported high-frequency CMOS SC filters.