University of Macau

Abstract

NON-SCAN DESIGN FOR TESTABILITY OF DIGITAL CIRCUITS BASED ON GENETIC ALGORITHM

by Ng Chi Long (Michael)

Student No.: M-97-6242-4

Thesis Supervisor: Mr. Farid Samandari and Dr. Peng Un Mak
Master of Science in Electrical and Electronics Engineering

Nowadays, the deep sub-micron Integrated Circuit (IC) manufacturing technology has made the ICs more and more complex. System on chip design now consists of hundreds of million transistors. The traditional IC test strategies cannot make proper test (low fault coverage) to such a huge circuit inside a chip due to the difficulty of justifying test sequences inputted to the system and propagating test response to the output of the system. New test schemes must be investigated to maintain the quality of a chip.

In order to reduce the cost and achieve Just In Time to market, efficient testing is considered in advance during the design phase – Design For Testability (DFT). In this work, multiplexer is used for observing some critical points inside the chip. The AND/OR gates are used to control the states of certain internal nodes. This can help the designer to make diagnosis of the circuit and to locate the problems when designing and debugging the circuit. During the test phase, since some internal nodes of the system can be observed and/or controlled, this DFT method simplified the test generation and test verification processes. It improves the fault coverage in testing the chip. In the way of test generation, Genetic Algorithm and Parallel Simulation are applied to search and obtain a test sequence which can optimize the fault coverage. The single stuck at faults are partitioned into subsets for parallel simulation. Examples of using DFT design combined with test generation using Genetic Algorithm are demonstrated which show that 100% fault coverage can be achieved.