ABSTRACT

WIDESPREAD utilization of multirate mixed analog and digital signal processing have increasingly created a great demand for design of accurate and high speed sampled-data analog (SDA) sampling rate converters, namely decimators and interpolators with high reliability and performance as well as efficiency in analog integrated circuitry with respect to the power and silicon consumption. Meanwhile, the currently developed design techniques for SDA interpolation give rise to undesired additional distortion in the overall system response due to the input lower sample-and-hold (S/H) filtering effect, hence downgrading the precision of not only the integer SDA interpolators but also both the rational SDA decimators and interpolators. Moreover, the relatively stringent speed requirement of output accumulators in previously developed multirate circuits also confines their potential for high speed operation.

This Thesis proposes a new design methodology of SDA sampling rate increase, which enables system performance to be no longer affected by the input S/H filtering effect, that is designated as Impulse Sampled technique and can be applied to SDA sampling rate converters which will become exactly equivalent to their digital counterparts. Both conventional bi-phase approach and specialized multirate techniques based on polyphase structures, with original prototype digital transfer function and without any modification as previously required are investigated for impulse sampled sampling rate conversion. Moreover, a complete, comprehensive family of impulse sampled integer interpolators and rational sampling rate converters, decimators and interpolators, realized with the state-of-the-art SC techniques are proposed with their novel individual and efficiently specialized design structures for both linear phase FIR and high-selectivity IIR responses. The impulse sampled parallel Direct-Form (DF) and Active-Delay Block (ADB), in canonic and non-canonic forms, polyphase structures are discussed for SC FIR interpolators with low and high-order filter responses, respectively. In addition, an efficient amplifier-shared recursive ADB polyphase structure with also canonic and non-canonic realization for SC IIR interpolators are proposed in both a single and multiple parallel stages realization. To achieve an higher sampling rate alteration factor with increased efficiency in analog circuitry, multistage implementations for both impulse sampled FIR and IIR interpolation are described with real design specification and consideration as well as critical design techniques of effective circuit customization. Finally, both impulse sampled FIR and IIR rational sampling rate converters are investigated with the conventional realizations and a more efficient and practical novel scheme – the Intermittent ADB Polyphase Structure with both single- and double-sampling techniques. Various SC effective circuit architectures for each of the design structures are proposed on the basis of the utilization of *L*-output-accumulator approach which has a considerable potential in high-frequency operation and one-output-accumulator approach which shows superiority in terms of the reduced number of circuit components, as well as of the input signal formats. All the circuit behavioral verifications are illustrated by exhaustive design examples with rigorous computer simulations. Experimental discrete-components SC realizations are also presented and they further demonstrate the practical feasibility and even the potential for future integrated circuit implementation in multirate mixed analog and digital signal processing systems.