

A **DECADE'S EFFORT** on lithography and integrated-circuit technologies has resulted in very low-cost low-power highly-integrated wireless systems. Entering in a network-ubiquitous era, not only such features continue as the design ambitions, but also the *multi-standardability* for optimum wireless connectivity; and the *low-voltage (LV) compliance* for facilitating the technology migration in sub-1-V nanoscale regimes.

This thesis proposes multistandard-compliant and LV analog-baseband techniques for the realization of emerging wireless communication systems. A coarse-RF fine-IF (two-step) channel-selection technique is disclosed. It, through the reconfiguration of receiver and transmitter analog basebands, enables not only a relaxation of the RF frequency synthesizer's and local oscillator's design specifications, but also an efficient multistandard compliance by synthesizing the low-IF and zero-IF in the receiver; and the direct-up and two-step-up in the transmitter.

The principle is demonstrated in the design of a system-in-a-package (SiP) receiver analog baseband for IEEE 802.11 a/b/g WLAN that is concurrently optimized for LV operation. It architecturally features: a unique 3D-stack floorplan and design methodology for high testability and routability; an IF channel selection and a flexible-IF reception for an optimum baseband signal conditioning of 802.11a/b/g. In the circuit level, three tailor-made LV-robust functional blocks are reinforced: 1) double-quadrature-downconversion filter (DQDF) – it realizes concurrently clock-rate-defined IF reception, I/Q demodulation, IF channel selection and baseband filtering; 2) switched-current-resistor (SCR) programmable-gain amplifier (PGA) – it offers a transient-free constant-bandwidth gain adjustment; 3) inside-OpAmp dc-offset canceler – it saves the silicon area required for realizing a large time constant on chip while maximizing its highpass-pole switchability for fast dc-offset transient.

Fabricated in a 3.3-V 0.35- μm CMOS process without resorting from specialized technology options, the analog baseband integrated in 3 mm² consumes 14 mW/channel at 1 V, while measuring 1- μs transient in a 52-dB gain step, 0.38- μs transient in IF channel selection, 32-dB (90-dB) stopband rejection ratio at 20 MHz (40 MHz) and 15.2-dBm IIP3.

Comparing with the previously reported LV (i.e., ≤ 1.5 V) continuous-time baseband building blocks, the realized DQDF and SCR PGA successfully extend the state-of-the-art boundary in terms of signal bandwidth and supply voltage. In addition, the entire analog baseband exposes the lowest-voltage, but power-competitive, analog-baseband solution for 802.11a/b/g-WLAN receivers ever reported.